Wahid Rahman

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SUMMARY OF QUALIFICATIONS

- 8 years research & industry experience in high-speed circuit design for CMOS & FinFET
- Co-author of 6 publications and 1 patent in the area of high-speed communication circuits
- Interested in research & development of next-generation data communication links

EDUCATION

University of California, Berkeley **Berkeley, California**
Ph.D. in Electrical Engineering Jan 2020 – Present
Research interest: Advanced optical communication links
Advisor: Prof. Vladimir Stojanovic
GPA: 4.00/4.00

University of Toronto **Toronto, Canada**
M.A.Sc. in Electrical & Computer Engineering Sep 2014 – Mar 2017
Thesis: Frequency Detection for Reference-less Baud-Rate CDR in 28nm CMOS
Advisor: Prof. Ali Sheikholeslami
GPA: 4.00/4.00 (Thesis: A+)

University of Toronto **Toronto, Canada**
B.A.Sc. in Engineering Science with Honours Sep 2009 – Jun 2014
Major in Electrical & Computer Engineering + PEY**
GPA: 3.88/4.00 Rank: 5th of 168 (Spring 2014)
**Professional Experience Year (14-month internship at Altera Corp., Toronto, Canada)

GRE: 170/170 Quantitative, 170/170 Verbal, 5.0/6.0 Analytical Writing Oct 2018

WORK & RESEARCH EXPERIENCE

Apple Inc., San Francisco, USA May – Dec 2021
Hardware Technology Intern

- Investigated new architectures for high-bandwidth I/O interfaces

Alphawave IP Inc., Toronto, Canada Sep 2017 – Dec 2019
Senior Analog/Mixed-Signal Design Engineer

- Employee #8 at SERDES startup with key design roles leading to USD $4.3 billion IPO
- Led original PLL designs with mentorship from founders for 112Gb/s transceivers in 7nm
- Conducted literature survey and proposed architecture for low-jitter >10GHz digital PLL
- Designed PLL circuits (phase interpolator, TDC, LC DCO), guided layout & digital teams, and conducted top-level mixed-signal sign-offs for successful tapeouts & silicon results

University of Toronto, Toronto, Canada Sep 2014 – Aug 2017
Graduate Research Student (Prof. Ali Sheikholeslami)

- Developed 28Gb/s baud-rate wireline receiver in TSMC 28nm (see ISSCC & JSSC 2017)

Altera Corporation, Toronto, Canada May 2012 – Jul 2013
Software/IP Development Intern (PEY)

- Designed PLL reconfiguration IP in Verilog with 10x LUT reduction for Arria 10 FPGAs
- Developed PLL models in C++ for use in Quartus CAD software for Arria 10 FPGAs

University of Toronto, Toronto, Canada May – Aug 2011
NSERC Undergraduate Research Student (Prof. Paul Chow)

- Investigated hybrid CPU/FPGA systems using MPI to accelerate real-time face detection
- Conducted data transfer bandwidth and latency tests between CPU and Xilinx FPGA

PUBLICATIONS & PATENTS

D. Yoo, M. Bagherbeik, **W. Rahman**, A. Sheikholeslami, H. Tamura, and T. Shibasaki, "A 36Gb/s Adaptive Baud-Rate CDR with CTLE & 1-tap DFE in 28nm CMOS," *IEEE Solid-State Circuits Letters*, pp. 252-255, Aug. 2019.

D. Yoo, M. Bagherbeik, **W. Rahman**, A. Sheikholeslami, H. Tamura, and T. Shibasaki, "A 30Gb/s 2x Half-Baud-Rate CDR," *CICC Proceedings*, pp. 1-4, Apr. 2019.

D. Yoo, M. Bagherbeik, **W. Rahman**, A. Sheikholeslami, H. Tamura, and T. Shibasaki, "A 36Gb/s Adaptive Baud-Rate CDR with CTLE & 1-tap DFE in 28nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 126-127, Feb. 2019.

W. Rahman, D. Yoo, J. Liang, A. Sheikholeslami, H. Tamura, T. Shibasaki, and H. Yamaguchi, "A 22.5-32Gb/s 3.2pJ/bit Reference-less Baud-Rate Digital CDR with DFE & CTLE in 28nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3517-3531, Dec. 2017 (**invited to Special Issue on ISSCC 2017**).

W. Rahman, D. Yoo, J. Liang, A. Sheikholeslami, H. Tamura, T. Shibasaki, and H. Yamaguchi, "A 22.5-32Gb/s 3.2pJ/bit Reference-less Baud-Rate Digital CDR with DFE & CTLE in 28nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 120-121, Feb. 2017.

S. Karimelahi, **W. Rahman**, M. Parvizi, N. Ben-Hamida, and A. Sheikholeslami, "Optical and Electrical Trade-offs of Rib-to-Contact Distance in Depletion-Type Ring Modulators," *OSA Optics Express*, vol. 25, no. 17, pp. 20202-20215, Aug. 2017.

W. Rahman, A. Sheikholeslami, T. Shibasaki, and H. Tamura, "CDR circuit and receiving circuit," US Patent No. 10,225,069, issued on Mar. 5, 2019.

PROFESSIONAL ACTIVITIES & AWARDS

NSERC CGS D, UC Berkeley (ranked 4th in Canada, EE subcommittee) 2020 – 2023
Reviewer, IEEE Journal of Solid-State Circuits, ISCAS, TCAS-II 2018 – 2021
EECS Departmental Fellowship, UC Berkeley 2020
ADI Outstanding Student Designer Award, Analog Devices Inc. 2017
Edward S. Rogers Sr. Graduate Scholarship, University of Toronto 2015 – 2017
NSERC Canada Graduate Scholarship (CGS M), University of Toronto 2015 – 2016
Ontario Graduate Scholarship (OGS), University of Toronto 2014 – 2015
Governor General's Bronze Academic Medal (Gov't. of Canada), Bell High School 2009