Awani Khodkumbhe | UC Berkeley

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Seeking summer 2023 internship in analog/mixed-signal, RF/mmWave ICs and wireless systems.

Education

Ph.D. University of California, Berkeley, Advisor: Prof. Ali Niknejad *Aug'21-present*
Major: Electrical Engineering and Computer Sciences CGPA: 3.91/4
Relevant Coursework: ICs for Communication, Advanced Analog ICs, Advanced Digital ICs and Systems
Minor: Business Administration
Relevant Coursework: Fundamentals of Business, Entrepreneurship

B.E. Birla Institute of Technology and Science (BITS), Pilani, Goa, India *Aug'16-Jul'20*
Major: Electronics and Instrumentation Engineering CGPA: 9.51/10, Dept. Rank 1

Industry Experience

Texas Instruments - Analog Design Engineer
Designed Under-Voltage Lockout (UVLO), Over-Voltage Lockout (OVLO) for isolated gate driver. *Aug'20 - Aug'21*

Texas Instruments - Analog Intern
Model parasitic extraction of passives at 14.5 GHz in 180 nm *May'19 - Jul'19*
- Using the de-embedded s-parameters, developed models of transmission line, MIM-capacitor, inductor, ISO-capacitor.

Research Experience

Integrated Circuit Design Group, University of Twente, The Netherlands - RFIC Intern
Design of mm-wave upconversion mixer at 26 GHz for a novel time-interleaved 5G New Radio *Feb'20 - Jul'20*
Advisors: Prof. Bram Nauta, Prof. Anne-Johan Annema
- Designed current-driven double-balanced linear passive mixer with I_{peak} = 46 mA in 22 nm CMOS FDSOI.
- The design consisted of bootstrapped switches and a transformer balun at the output.

Preserving polar modulated class-E power amplifier(PA) linearity under load mismatch *Aug'19 - Dec'19*
Advisors: Prof. Bram Nauta, Prof. Anne-Johan Annema
- Implemented a system of polar class-E PA with an on-chip waveform characterizer in 22 nm CMOS FDSOI enabling automatic adaptive digital predistortion (ADPD).
- Corrected AM/AM, AM/PM distortion, memory and temperature effects under load mismatch of VSWR up to 9:1.
- Performed load-pull measurements for a 2 GHz 1024 QAM signal with 1 MSym/s symbol rate.
- Demonstrated RMS EVM $\leq$ 1.5% and ACPR $\leq$ -35 dB maintained in a significantly larger area on the Smith chart going from 50 Ω optimized static DPD to our ADPD.

Publications

A. Khodkumbhe, M. Huiskamp, A. Ghahremani, B. Nauta, A.J. Annema, "Preserving Polar Modulated Class-E Power Amplifier Linearity under Load Mismatch", IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2020. Full-text invited for IEEE Transactions on Microwave Theory and Techniques (T-MTT). Online Full-Paper Access

Technical Skills

Cadence Virtuoso, SPICE, MATLAB, Simulink, LabVIEW, ADS, Eagle PCB, C, Verilog, Assembly Language

Academic Projects

Design of DAC driver transimpedance amplifier (TIA) *Apr'22*
- Designed a fully differential 2-stage OpAmp with gain-boosting, Ahuja compensation, common-mode feedback.
- Loopgain = 65.5 dB, BW = 531 MHz, PM = 60.2°, settling time = 2.9 ns, power = 4.8 mW, output noise = 160 uVrms.

Design of RF mixer for zero-IF receiver *May'20 - Jul'20*
- Designed single-balanced active mixer in 65 nm CMOS for ISM band at 2.4 GHz.
- Voltage gain = 11 dB, IIP_3 = 3.5 dBm, NF = 10 dB, power = 2.4 mW.

Awards

- Selected for NSF funded IEEE IMS Project Connect. *Mar'22*
- Selected for UC Berkeley, Stanford, MIT highest fellowships. *Apr'21*