YUE **DAI**

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EDUCATION

University of California, Berkeley – Berkeley, California, United State (09.2018 -)

- Ph.D candidate in Electrical Engineering
- M.S in Electrical Engineering (05.2021)

University of Michigan – Ann Arbor, Michigan, United State (09.2016 - 04.2018)

- B.S in Electrical Engineering
- Overall **GPA: 3.92**

Shanghai Jiaotong University – Shanghai, China (09.2014 - 06.2016)

- B.S in Electrical and Computer Engineering
- Overall **GPA: 3.83**, rank top 10 in college

RESEARCH AREA

Digital Signal Processing, Computer Architecture, VLSI design

RESEARCH

A Scalable Massive MIMO Baseband DSP RTL Design (10.2018 -)

- Design the system datapath and implement individual modules in Chisel and hookup on Rocketchip.
- Test individual models using random test and the integrated datapath against python system simulator.
- Fully parameterizable on numbers of antennas and users in the system, and the scale of parallelization.

***Snappy* Compression Accelerator on Rocket Core (1.2019 - 5.2019)**

- Design and implement *Snappy* compression algorithm in Chisel as an accelerator of Rocket core.
- The hardware accelerator is capable of compressing data up to 100 times faster than software, at the cost of a slightly decreased compression ratio.

Wifi Bi-directional Back-Channel Communication System (01.2017 - 10.2017)

- Realize the communication between Ultra Low Power devices and commercial wifi infrastructures.
- Design and implement real-time bi-directional communication system using USRP.
- Sensitivity level back-channel communication system is -94dBm received signal power.

2-way Superscalar MIPS R10K Processor (02.2017 - 05.2017)

- Design and implement a 2-way superscalar OoO processor using R10K structure including fast branch recovery, set-associative cache and load-to-store forwarding load store queue.
- Synthesize and analyze the performance of R10K processor.
- Successfully increase CPI and clock frequency.

TEACHING EXPERIENCE AND INTERNSHIP

GSI for CS252 Computer Architecture (01.2020-06.2020)

CPU Architecture Research in *Futurewei Technologies, Inc* (06.2020-08.2020)

- RSIC-V vector unit design and implementation for Whitney CPU

PUBLICATION

- **Yue Dai,** Harrison Liew, et al. “A Scalable Generator for Massive MIMO Baseband Processing Systems with Beamspace Channel Estimation”, *2021 IEEE SiPS,* 2021.
- **Yue Dai,** Greg LaCaille, Harrison Liew, et al. “A Scalable Massive MIMO Uplink Baseband Processing Generator”, *2021 IEEE ICC*, Montreal, 2021.
- **Yue Dai**, Wenhao Peng, Yu Wang, et al. “Implementation and Evaluation of Bi-directional WiFi Back-channel Communication.” *2018 IEEE 29th PIMRC*, Bologna, 2018.