

SUMMARY

- 9+ years of research and industry experience in high-speed serial link design and analysis
- Area of expertise include system-level SerDes link modeling, statistical analysis, DSP-based non-linear equalizer design, and analog & microwave circuit design
- Looking for system-level SerDes architect or AMS circuit design role for the development of 100+ Gbaud/s electrical or optical communication link

EDUCATION

University of California, Berkeley	<i>Expected Dec. 2024</i>
<i>Ph. D. in Electrical Engineering; Advisor: Dr. Elad Alon and Dr. Ali Niknejad</i>	Berkeley, CA
<i>Winner of 2022 Qualcomm Innovation Fellowship (One of 19 winners among 132 participants)</i>	
California Institute of Technology (Caltech)	<i>Graduated in Jun. 2014</i>
<i>M.S. in Electrical Engineering; Advisor: Dr. Azita Emami</i>	Pasadena, CA
Texas A&M University	<i>Graduated in Dec. 2011</i>
<i>B.S. in Electrical Engineering; Advisor: Dr. Jose Silva-Martinez and Dr. Samuel Palermo</i>	College Station, TX
<i>Graduated with Summa Cum Laude, University Honors, and Undergraduate Research Fellow Award</i>	

PUBLICATIONS AND PATENTS

- **Kunmo Kim et al.**, "Precursor ISI Cancellation Sliding-Block DFE for High-Speed Wireline Receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 10, pp. 4169-4182, Oct. 2023.
- **Kunmo Kim et al.**, "Accurate Statistical BER Analysis of DFE Error Propagation in the Presence of Residual ISI," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 2, pp. 619-623, Feb. 2022.
- **Kunmo Kim et al.**, "Baseline Wander Correction in AC Coupled Communication Links using Equalizer with Active Feedback," #US10833898B2, Nov 2020. (Primary Contributor)
- **Kunmo Kim and J. Silva-Martinez**, "Low Power 3rd-Order Continuous-Time Low-Pass Sigma-Delta Analog- to-Digital Converter for Wideband Applications," *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp. 814-817.

ACADEMIC RESEARCH EXPERIENCE DURING PHD JOURNEY

ADC-based SerDes with Advanced Non-Linear Equalizer for 128 Gbaud/s in Intel 16 nm	<i>UC Berkeley, CA</i>
– Developed two novel non-linear feed-forward equalizers. The proposed equalizers have zero concern about the loop timing constraint and outperform a conventional sub-optimal EQ (i.e., FFE + DFE) – Developed a system-level analysis tool and EQ adaptation algorithms for the advanced non-linear equalizers – Currently working on CTLE, current-integrating track-and-hold, and time-domain ADC for the next-generation power-efficient ADC-based SerDes link	
Wideband Matching Network Design for 100+ Gbaud/s SerDes in Intel 16 nm	<i>UC Berkeley, CA</i>
– Designed a wide-bandwidth impedance matching network achieving state-of-the-art performance – BW = 75 GHz, RL < -10 dB from DC~65 GHz, group delay variation < 3 ps from 100 MHz~100 GHz – Satisfies ESD compliance voltage requirements for the 125 V CDM event – Completed and simulated 3D EM model of chip interfaces including on-chip impedance matching networks, C4 pads, copper pillars, and a package interposer structure using HFSS	
Development of Accurate Statistical Analysis of DFE Error Propagation Effect	<i>UC Berkeley, CA</i>
– Identified logical errors found in literature and proposed precise statistical model of DFE – Proposed multi-variable Markov chain model to accurately capture the error propagation behavior of the DFE in the presence of residual ISI – Proposed an accurate closed-form equation for the expected burst error length of the DFE error propagation	
Development of Statistical Analysis Tool for High-Speed SerDes Link	<i>UC Berkeley, CA</i>
– Implemented statistical models of various components for the rapid analysis of link margin: channel, on-chip matching network, Tx & Rx FFE, CTLE, DFE, CDR, FF-MLSE, and various noise and jitter effects – The framework is written in Python and supports PAM 2, 3, and 4 modulation. The results are compatible to the COM model from IEEE 802.3 standard	

INDUSTRY EXPERIENCE

Apple

Oct. 2017 - Aug 2018 (1 yr.)

Full-Time SerDes Circuit Design Engineer

Cupertino, CA

- Developed DFE circuits and adaptation algorithm for 80 Gbps Thunderbolt. Specifics restricted by NDA.

Oracle

Jul. 2014 - Sep. 2017 (3 yr.)

Full-Time SerDes Circuit Design Engineer

Santa Clara, CA

- Designed a frequency-modulation-insensitive DLL for 32 Gb/s SerDes receiver clock distribution network
- Designed an active-feedback-based CTLE and associated PVT-invariant biasing circuit with customized inductors for 32 Gb/s SerDes receiver in 7 nm FinFET for Infiniband EDR and PCIe 5.0 standard
- Invented a baseline-wander correction filter integrated with a CTLE (USPTO #US10833898B2)
- Proposed and designed a new replica-based VGA minimizing gain variation against PVT corners
- Designed low-loss and low group delay variation wide-band impedance matching networks and internal loopback receivers. Design is simulated via Sonnet (3D EM structure simulator)

Qualcomm

Feb. 2012 - July. 2013 (1.5 yr.)

Full-Time Bench Test Engineer

San Diego, CA

- Developed test characterization methodology and software framework for V/I-ADCs, battery charging modules, and Buck+LDO voltage regulators of PMIC products (PM8941, PM8841, PM8019)

National Instruments

May. 2011 - Aug. 2011 (3 mo.)

Interim Analog Hardware Engineer

Austin, TX

- Designed current-feedback OPAMP-based variable gain ADC driver, 20 MHz noise filter, and 40 MHz anti-aliasing filter for a high-resolution modular oscilloscope product for PXI chassis (NI PXI-5142)
- Each design is fully characterized and verified in the lab. The final designs are successfully merged into the product (NI PXI-5142)

REFERENCES

Ali Niknejad; Ph.D. Advisor, Dept. EECS, UC Berkeley.

✉ niknejad@berkeley.edu

Elad Alon; Ph.D. Advisor, Dept. EECS, UC Berkeley.

✉ elad@bcanalog.com

Azita Emami; M.S. Advisor, Dept. EE, Caltech.

✉ azita@caltech.edu

Jose Silva-Martinez; B.S. Advisor, Dept. EE, Texas A&M Univ.

✉ jose-silva-martinez@tamu.edu

Samuel Palermo; B.S. Advisor, Dept. EE, Texas A&M Univ.

✉ spalermo@tamu.edu

Kenneth Arcudia; Senior Director of Technology, Qualcomm.

✉ karcudia@qti.qualcomm.com

Sanjeev Maheshwari; Senior Manager of SerDes Design Group, Apple.

✉ sanjeevm@apple.com

Dawei Huang; Director of Analog and Mixed-Signal Circuit Design Group, Oracle.

✉ dawei@sambanova.ai