Yikuan CHEN

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EDUCATION BACKGROUND

Aug.2018 – Present
(Expected Dec 2024)

University of California, Berkeley

MS/Ph.D. student in **Electrical Engineering**

GPA: **3.96/4.0**

Current Graduate Student Researcher at Berkeley Wireless Research Center (BWRC)

Aug.2014 – May 2018

University of Illinois at Urbana Champaign

Bachelor of Science, Major in **Electrical Engineering** & Minor in **Physics and CS**

Overall GPA: **3.97/4.0**

INTERNSHIPS

May 2023 - Aug. 2023

Apple Inc (Cupertino) *Wireless System Research Engineer Intern*

- Implementing mmWave test device controller
- mmWave radar sensing tests
- mmWave sensing channel modeling

May 2021 - Aug. 2021

Apple Inc (Cupertino) *Hardware Engineer Intern*

- mmWave frontend module HFSS simulation
- Phase-noise measurement automation

May 2020 - Aug. 2020

Apple Inc (Cupertino) *Hardware Engineer Intern*

- mmWave microwave design
- Data analysis on PVT

CALTERAH Semiconductor Co., Ltd. (SHANGHAI) *Hardware Engineer Intern*

Jul. 2018

- Multi-sensor fusion for Autonomous Driving

Individually developed the camera+FMCW visualization for vehicle recognition & tracking

- Developed a GUI to project the radar results onto the camera view
- Invented a method with GUI to very quickly calibrate the projection transformation
- Patent applied and published in China National Intellectual Property Administration (CN109118537A)

Jul. 2017 – Aug. 2017

- FMCW Backend Development on MCU

Individually developed the low cost MCU-based backend system for commercial FMCW radar

- Designed and developed a 1D multiple-slope FMCW scanning control
- Realized computationally efficient FFT, OS-CFAR, DOA Estimation and tracking algorithm
- Successfully optimized the algorithms to achieve more moderate performance (up to 10 target tracking) but much lower price than the FPGA+ARM-Core based solution

May 2016 – Aug. 2016

➢ IP Core Development for Millimeter-wave Radar

Teamwork developed a fixed point configurable FFT IP core on FPGA for a Millimeter-wave radar

- Studied a variety of FFT algorithms with different radix, architecture, number types
- Prototyped in C++ with own-developed fixed-point library
- Implemented pipelined algorithm on FPGA with radix-2, up to 1024-point CFFT

AWARDS & HONORS

May. 2024 Best Student Poster for "140GHz FMCW Radar with RF Leakage Cancellation" in 2024 BWRC Annual Research Review

Mar. 2023 UC Berkeley 2023 Outstanding Graduate Student Instructor Award

Apr. 2018 University of Illinois Bronze Tablet Award –*Top 3% students*

Apr. 2018 HKN Outstanding Senior Student Award ($500)

Nov.2017 Horace and Kate King Wu International Undergraduate Scholarship ($1,000)

Sep.2017 Omron Electrical Engineering Scholarship ($3,750) - *Top 0.3%*

Aug.2015 – May 2018 UIUC James Scholar (University level)

Dec.2014 – Jun. 2015 UIUC Dean's List of College of LAS – *Top 10%*

Dec.2015 – Jun. 2017 UIUC Dean's List of College of Engineering – *Top 10%*

RESEARCH EXPERIENCES AND PROJECTS

Oct. 2021 - Present

Next Generation 140GHz Radar for Gesture Recognition

140GHz FMCW radar for short-range gesture recognition with phase noise cancellation

- Taped out an FMCW radar chip with 10GHz bandwidth at 140GHz
- Proposed and designed self-interference and leakage cancellation method in RF domain
- Designed and fabricated the package with different antenna-on-package configurations
- Designed PCBs for bringing up the chip and full radar system
- Designed and implemented FPGA digital subsystem for data conversion, FFT and leakage cancellation loop control

Aug. 2018 - Oct. 2021

Wideband Transmitter for mm-Wave Digital Arrays

mm-Wave Transmitter with high linearity and wideband from 20GHz to >70GHz

- Explored the design space between traditional DAC+Mixer solution and distributed RF-DAC
- Designed a high linearity active mixer with flattened gain across large DAC output range
- Taped out the test chip for the mixer in 28nm (October 2019)
- Designed a wideband DAC with 1GHz IF bandwidth, oversampled to 10GHz
- Taped out the test chip for the Tx in 28nm (April 2021)

Aug.2017 – May.2018

Sound classification using CNN-LSTM neural network (Undergraduate Senior Thesis)

Developed a 2D CNN+LSTM neural network to perform sound classification

- Studied different sound localization algorithms and sound enhancement schemes
- Implement accumulated correlation for sound localization and generalized-sidelobe-cancellation for sound quality enhancement
- Using DNN to perform sound classification

- Minimizing the power consumption by algorithm optimization and using low power HDL coding

Digital IC and VLSI course projects

Nov.2017 – Dec.2017

➢ Read-out Circuitry for an On-chip sensor array

A circuit for communication with off-chip diagnostic system using serial in/out port

- Designed and constructed the circuit layout using 45 nm technology
- Main logic operates at 2GHz/1.1V and I/O operates at 20MHz/1.8V
- Performed post layout simulation and minimized power consumption using low-power design

➢ Clone of AMD Am2901

A complete layout of Am2901 microprocessor using Cadence Virtuoso

- Full custom layout for data path and automated synthesize for controller

Aug. 2016 – Dec.2016

FPGA-based SoC Arcade Game (Course Project - *Top 3/300*)

A two-player game running on Altera Cyclone IV FPGA (developed in Quartus and Eclipse)

- Designed the framework of game and determined the software & hardware co-design pattern
- Used SystemVerilog to implement the game logic and functions including sine motion, score board, scrolling screen, sprite, FPGA-controlled AI enemy
- Improved the functions by implementing movement control, boundary test, barrier recognition etc.

Extra-curricular Activities

Jan. 2022 – Dec. 2022

Graduate Student Instructor in EECS151/251A (Intro. to Digital Design and IC)

- Taught discussion sessions and FPGA labs
- Made video tutorials to help students understand concepts in the course
- Developed the "UART, FIFO & Memory Controller" FPGA lab

Jan. 2017 – May 2018

Teaching Assistant of ECE 385 in Digital System Laboratory (15h office hours/week)

- Helped students with Lab and projects about FPGA and TTL circuits
- Record tutorial video for SystemVerilog with Quartus and ModelSim
- Held exam review sessions

Jan. 2017 – May 2018

Founder and Builder of Technical Website (http://kttechnology.wordpress.com)

- Helped over 300 students understanding lab material, getting help with final project and exams
- Over 15,000 views in Spring 2017 semester by ECE 385 students; over 90,000 views by Nov. 2019 by viewers from 33 countries/regions in the world

Skillset

- **Excellent with:**

C, C++, MATLAB, Python, SystemVerilog/Verilog, HSPICE | Quartus, ModelSim, Vivado, Cadence Virtuoso, ADS, Ansys HFSS, Altium

- **Proficient in:**

Linux, UNIX | PSPICE| DMM, Realtime/Sampling Oscilloscope, VSA, VNA

- **Experienced with:**

x86 Assembly | SoC design with FPGA | Soldering | Network Programming, System Programming

Miscellaneous

- Composed 24 pieces of music (using Overture 4.0), including one 12-track symphony, since 2013
- Published 70,000-word science fiction in 2011 and 5,000-word economic essay on Chinese Commercial Times in 2013.