CHANGUK LEE

Ph.D., Mixed-signal circuit designer

Dept. of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea

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RESEARCH INTERESTS

Analog/Mixed signal circuit, data converters (ADC, DAC), precision analog, low-noise sensor interface (Bio-medical, Imager), and miniaturized wireless neural interface.

EDUCATION

Yonsei University, *Seoul, South Korea*

- Ph.D. in Electrical and Electronic Engineering Mar. 2017 – Aug. 2022
  (Supervisor: Prof. Youngcheol Chae)
  - Dissertation title: Energy Efficient, Miniaturized Wireless Neural Recording System
- B.S. in Electrical and Electronic Engineering Mar. 2009 – Aug. 2016

RESEARCH EXPERIENCE

University of California, Berkeley, *CA, USA*

- Postdoctoral Scholar – EECS Department & BWRC
  (Supervisor: Prof. Rikky Muller) March 2023 – Present

Yonsei University, *Seoul, South Korea*

- Postdoctoral Fellow – Institute of Industrial Technology
  (Supervisor: Prof. Youngcheol Chae) Sep. 2022 – Feb. 2023

Stanford University, *CA, USA*

- Visiting Student Researcher: Participated in Retina Project
  (Supervisor: Prof. Boris Murmann) Sep. 2019 – Feb. 2020

PUBLICATIONS

Conference Papers

[C12] M. Jang, W.H. Yu, **C. Lee**, M. Hays, P. Wang, N. Vitale, P. Tandon, P. Yan, P.I. Mak, Y. Chae, E.J. Chichilnisky, B. Murmann, and D.G. Muratore, “A 1024-Channel 268 nW/pixel 36x36 μm^2/ch Data-Compressive Neural Recording ICf or High-Bandwidth

Brain-Computer Interfaces," *IEEE Symposium. On VLSI Circuits (**SOVC**)*, June 2023.

[C11] J. Yoon, M. Jang, **C. Lee**, Y. Lim, and Y. Chae, "A 243μW 97.4dB-DR 50kHz-BW Multi-Rate CT Zoom ADC with Inherent DAC Mismatch Tolerance," *IEEE Custom Integrated Circuits Conference (**CICC**)*, April 2023.

[C10] **C. Lee**, B. Kim, J. Kim, S. Lee, T. Jeon, W. Choi, S. Yang, J. Ahn, J. Bae, and Y. Chae, "A Miniaturized Wireless Neural Implant with Body-Coupled Data Transmission and Power Delivery for Freely Behaving Animals," *IEEE International Solid-State Circuits Conference (**ISSCC**)*, Feb. 2022.

[C9] H. Lee, **C. Lee**, J. Lee, Y. Choi, and Y. Chae, "A 0.033mm^2 21.5-aF Resolution Continuous-Time Delta-Sigma Capacitance-to-Digital Converter with Parasitic Capacitance Immunity Up to 480pF," *IEEE Asian Solid-State Circuits Conference (**A-SSCC**)*, Nov. 2021.

[C8] Y. Lee, B. Cho, **C. Lee**, J. Kim, and Y. Chae, "A 47.5nJ Resistor-to-Digital Converter for Detecting BTEX with 0.06ppb-Resolution," *IEEE Symposium. On VLSI Circuits (**SOVC**)*, June 2021.

[C7] Y. Chae, M. Jang, **C. Lee**, S. Lee, and S. Song, "A Negative R-Assisted Amplifier on the Virtual Ground and Its Applications," *IEEE Custom Integrated Circuits Conference (**CICC**)*, April 2021.

[C6] J. Kwon, **C. Lee**, Y. Chae, and B. Murmann, "Design Considerations for External Compensation Approaches to OLED Display Degradation," *IEEE International Symposium on Circuits and Systems (**ISCAS**)*, Oct. 2020.

[C5] **C. Lee**, T. Jeon, M. Jang, S. Park, Y. Huh, and Y. Chae, "A 6.5μW 10kHz-BW 80.4dB-SNDR Continuous-Time ΔΣ Modulator with G_m-input and 300mV_{pp} Linear Input Range for Closed-loop Neural Recording," *IEEE International Solid-State Circuits Conference (**ISSCC**)*, Feb. 2020.

[C4] M. Jang, **C. Lee**, and Y. Chae, "A 134μW 24kHz-BW 103.5dB-DR CT ΔΣ Modulator with Chopped Negative-R and Tri-level FIR DAC," *IEEE International Solid-State Circuits Conference (**ISSCC**)*, Feb. 2020.

[C3] Y. Kim, S. Park, S. Song, S, Lee, M. Jang, **C. Lee**, and Y. Chae, "A 41μW 16MS/s 99.2dB-SFDR Capacitively Degenerated Dynamic Amplifier with Nonlinear Slope Factor Compensation," *IEEE International Solid-State Circuits Conference (**ISSCC**)*, Feb. 2020.

[C2] S. Song, **C. Lee**, M. Jang, and Y. Chae, "A 185μW -105.1dB THD 88.6dB SNDR Negative-R Stabilized Audio Preamplifier," *IEEE European Solid-State Circuits Conference (**ESSCIRC**)*, Sept. 2019.

[C1] **C. Lee**, M. Jang, and Y. Chae, "A 1.2V 68μW 98.2dB-DR Audio Continuous-Time Delta-Sigma Modulator," *IEEE Symposium. On VLSI Circuits (**SOVC**)*, June 2018.

Journal Papers

[J7] H. Yoon, **C. Lee**, T. Kim, Y. Kwon, and Y. Chae, "A 65 dB-SNDR Pipelined SAR ADC using PVT-Robust Capacitively-Degenerated Dynamic Amplifier," *IEEE Journal of Solid-State Circuits (**JSSC**)*, Accept.

[J6] **C. Lee**, B. Kim, J. Kim, S. Lee, T. Jeon, W. Choi, S. Yang, J. Ahn, J. Bae, and Y. Chae, "A Miniaturized Wireless Neural Implant with Body-Coupled Data Transmission and Power Delivery for Freely Behaving Animals," *IEEE Journal of Solid-State Circuits (**JSSC**)*, Vol. 57, No. 11, pp. 3212 - 3227, Nov. 2022. **Special Issue – Invited from *ISSCC* 2022**.

[J5] Y. Lee, B. Cho, **C. Lee**, J. Kim, and Y. Chae, "A 0.5 ms 47.5 nJ Resistor-to-Digital Converter for Resistive BTEX Sensor Achieving 0.1-to-5-ppb Resolution," *IEEE Journal of Solid-State Circuits (**JSSC**)*, Accept.

[J4] H. Lee, **C. Lee**, I. Lee, and Y. Chae, "A 0.033-mm^2 21.5-to-119.4-aF Resolution Continuous-Time ΔΣ Capacitance-to-Digital Converter Achieving Parasitic Capacitance Immunity up to 480-pF," *IEEE Journal of Solid-State Circuits (**JSSC**)*, Vol. 57, No. 10, pp. 3048 - 3057, Oct. 2022.

[J3] M. Jang, **C. Lee**, and Y. Chae, "A 134-μW 99.4-dB SNDR Audio Continuous-Time Delta-Sigma Modulator with Chopped Negative-R and Tri-level FIR DAC" *IEEE Journal of Solid-State Circuits (**JSSC**)*, Vol. 56, No. 6, pp. 1761 - 1771, June 2021.

[J2] **C. Lee**, T. Jeon, M. Jang, S. Park, J. Kim, J. Lim, J. Ahn, Y. Huh, and Y. Chae, "A 6.5μW 10kHz-BW 80.4dB-SNDR G_m-C Based CT ΔΣ Modulator with Feedback-Assisted G_m Linearization for Artifact-Tolerant Neural Recording," *IEEE Journal of Solid-State Circuits (**JSSC**)*, Vol. 55, No. 11, pp. 2889 - 2901, Nov. 2020. **Special Issue – Invited from *ISSCC* 2020**.

[J1] M. Jang, **C. Lee**, and Y. Chae, "Analysis and Design of Low-Power Continuous-Time Delta-Sigma Modulator Using Negative-R Assisted Integrator" *IEEE Journal of Solid-State Circuits (**JSSC**)*, Vol. 54, No. 1, pp. 277 - 287, Jan. 2019.

Patents

[P3] Y. Chae and **C. Lee**, "Analog-to-Digital Converter," Korea Patent 10-2022-0058762, 2022.

[P2] J. Bae, Y. Chae, B. Kim, **C. Lee**, "Apparatus for Wireless Neural Interface System," Korea Patent 10-2022-0024951, 2022.

[P1] Y. Chae, Y. Lee, and **C. Lee**, "Energy-Efficient Resistance-to-Digital Converter," Korea Patent 10-2021-0044403, 2021.

HONORS & AWARDS

[A7] **Grand Prize (1st), BK21+ Outstanding Graduate Students**,
by Yonsei University. Mar. 2022

[A6] **Gold Prize (1st), Samsung Human-Tech Paper Award**,
by Samsung Electronics. Feb. 2022

[A5] **IEEE SSCS Student Travel Grant Award (STGA)**,
by International Solid-State Circuits Conference (ISSCC). Feb. 2022

[A4] **IEEE SSCS Pre-Doctoral Achievement Award**,
by IEEE Solid-State Circuits Society (SSCS). Feb. 2022

[A3] **Silver Prize, Samsung Human-Tech Paper Award**,
by Samsung Electronics. Feb. 2020

[A2] **Bronze Prize, Samsung Human-Tech Paper Award**,
by Samsung Electronics. Feb. 2018

[A1] **Honor Student Award**, by Yonsei University. Feb. 2016

RESEARCH HIGHLIGHTS

Energy-Efficient Analog-to-Digital Converter for Audio Application

- The prototype is implemented in a 65-nm CMOS process.
- Key concept: A CT-ΔΣM using negative-R assisted integrator and tri-level feedback RDAC.
- Achieving 98.2 / 94.1-dB DR / SNDR in 24-kHz bandwidth while consuming 68-μW.
- Achieving state-of-the-art energy efficiency: Schreier's FoM_{DR} of 183.6-dB.
- Presented in *IEEE Symposium on VLSI Circuits (SOVC)* 2018 [C1] and published in *IEEE Journal of Solid-State Circuits (JSSC)* 2019 [J1].
- Awarded in Samsung Human-Tech Paper Award (Bronze Prize) [A2].

Energy-Efficient Analog-to-Digital Converter for Closed-Loop Neural Recording

- The prototype is implemented in a 110-nm CMOS process.
- Key concept: A CT-ΔΣM using Feedback-Assisted G_m Linearization at the G_m-C integrator.
- Achieving 300-mV_{pp} range, 80.4-dB SNDR in 10-kHz BW while consuming 6.5-μW.
- Achieving state-of-the-art energy efficiency: Schreier's FoM_{SNDR} of 172.3-dB.
- Presented in *IEEE International Solid-State Circuits Conference (ISSCC)* 2020 [C5] and invited to be published in *IEEE Journal of Solid-State Circuits (JSSC)* 2020 [J2].

Fully Integrated, Miniaturized Wireless Neural Recording System

- The prototype is implemented in a 110-nm CMOS process.
- Key concept: The first neural implant using body-coupled wireless power/data transmission.
- Achieving 644-μW wireless power recovery and 20.48-Mb/s data rate at the state-of-the-art energy efficiency of 32-pJ/b.
- End-to-end functionality validated through *in-vivo* experiments on freely moving rat.
- Presented in *IEEE International Solid-State Circuits Conference (ISSCC)* 2022 [C10] and invited to be published in *IEEE Journal of Solid-State Circuits (JSSC)* 2022 [J6].
- Awarded in Samsung Human-Tech Paper Award (Gold Prize – 1st) [A6].

REFERENCES

- Prof. Rikky Muller, Electrical Engineering and Computer Science (EECS), UC Berkeley, CA, USA, rikky@berkeley.edu.
- Prof. Youngcheol Chae, Electrical and Electronic Engineering, Yonsei University, Seoul, Korea, ychae@yonsei.ac.kr, (+82) 2-2123-2866.
- Prof. Boris Murmann, Electrical Engineering, Stanford University, CA, USA, murmann@stanford.edu.