Antroy Roy Chowdhury

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Research Interests

- Silicon-Photonic Integrated Circuits
- Circuits for High-Speed Wireline Links
- Analog and Mixed-Signal VLSI Circuit Design

Education

University of California, Berkeley, *CA, USA*
Doctor of Philosophy in Electrical Engineering and Computer Science (EECS) *Aug. 2020 – Present.*
GPA: **3.962 / 4**

Indian Institute of Technology, Kharagpur, *West Bengal, India*
Bachelor and Master of Technology (Dual-Degree) in Electronics and Electrical Communication Engineering
Master's specialization in Microelectronics and VLSI Design *Jul. 2015 – Apr. 2020*
Cumulative GPA: **9.78 / 10**
Topper of the Specialization ; *Rank-2* in the Department ; *Rank-4* in the Institute

Publications

Conference

- **A. Roy Chowdhury**, N. Wary and P. Mandal, "A Regulated-Cascode Based Current-Integrating TIA RX with 1-Tap Speculative Adaptive DFE", *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, TX, USA, 2019, pp. 790-793.
- **A. Roy Chowdhury**, N. Wary and P. Mandal, "Energy Efficient Bidirectional Equalized Transceiver with PVT Insensitive Active Termination," *2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID)*, Delhi, NCR, India, 2019, pp. 25-30.

Journals

- **A. Roy Chowdhury**, S. Maity and S. Sen, "Theoretical Analysis of Multi Integrating RX Front-Ends for Lossy Broad-Band Channels", in *IEEE Open Journal of Circuits and Systems*, vol. 2, pp. 363-379, 2021.
- N. Wary, **A. Roy Chowdhury** and P. Mandal, "Hybrid Bidirectional Transceiver for Multipoint-to-Multipoint signaling across On-Chip Global Interconnects", *IET Circuit, Devices and System*, Vol.14, Issue 6, pp. 780-787, Sept. 2020.

Industry Experience

Ayar Labs Inc. *Emeryville, CA, USA* May. 2024 – Aug. 2024
[*Internship*] *Advanced Electro-Optic Measurement Techniques for a 2 Tbps TeraPHY Optical Transceiver Module*
- Testing firmware development for micro-ring resonator (MRR) based 8λ DWDM link with an aggregate transceiver bandwidth of 2Tbps.
- Investigation into the electronic and photonic building blocks for MRR based 8λ DWDM link (TeraPHY) in monolithic CMOS-SOI process.

Mediatek Inc., *Irvine, CA, USA* May. 2023 – April. 2024
[*Internship*] *Circuits for High-Speed Silicon Photonic Transceivers*
- Designed the transmitter path for a 448 Gb/s/λ coherent electro-optic transceiver.
- Designed Mach-Zehnder Modulator driver circuits for 112 Gb/s PAM4 data transmission.

Apple Inc., *Cupertino, CA, USA* May. 2022 – Aug. 2022
[*Internship*] *RX-AFE Design for Advanced SerDes*

- Worked on codifying the design methodology of RX analog front-end (AFE) building blocks for 64Gbps PAM4 links for PCIe6.
- Explored different bandwidth-extension schemes for ultra high-speed RX.

Academic Internships

Design and Analysis of Integrating RX Front-Ends for Lossy Broad-band Channels, *Purdue University, West Lafayette, IN, USA* May. 2019 – July. 2019
Advisor: Prof. Shreyas Sen

- Carried out a rigorous theoretical analysis of different integrating RX front-ends employed in broad-band communications through lossy "wireline-like" channels (typical example being proximity communication and human-body communication), where simultaneous high integrated noise and low signal-swing limits the maximum achievable data-rate for a target bit-error rate (BER) and deteriorates the energy-efficiency of the RX. Obtained transient, noise and gain performance of different standard signaling blocks with closed-form expressions. Multi-integrator cascade has been proposed which provides significant gain with relatively lower power consumption than the standard gain elements. Also, maximum achievable data-rate and optimum energy efficiency for different channel losses have been obtained theoretically for different architectures revealing their advantages and limitations. All the pertaining circuits have been designed in 65nm CMOS process with a 1 V supply voltage.

Design and Study of Digital-to-Time Converters (DTCs) and Phase-Interpolators (PIs), *The University of British Columbia, Vancouver, Canada* May. 2018 – July. 2018
Advisor: Prof. Sudip Shekhar

- Executed a thorough literature survey on the state-of-the art digital-to-time converters (DTC) and phase-interpolators (PI), whose applications include, but not limited to, fractional-N PLLs, ADPLLs, clock and data recovery (CDR) circuits, polar transmitters etc. DTC architectures, based on delay-lines, variable-slope and constant-slope methods and PI architectures, including DLL based, signal-superposition based and charge-based PI cells, have been explored in detail.
- Proposed a novel charge-injection based digital-to-phase converter (CI-DPC) which utilizes the phase-shift property of a free-running LC-VCO on injecting a finite amount of external charge into it. The proposed CI-DPC achieves a full-2π phase-shift range with 12-bit resolution and having a simulated peak-DNL of 0.0055^o. The entire system is designed in 65nm CMOS technology consuming a total power of 3.11mW from a 1.2V and 2.5V supply.

Advanced VLSI Summer School, *Indian Institute of Technology, Kharagpur, India* May. 2017 – June. 2017

- Analog VLSI: Complete design flow from circuits and codes to full chip layout; analog front-end design for sensor data acquisition in biomedical applications and neural interfaces; Different amplifier and filter topologies, CMFB, stability, compensation, power management, energy-harvesting.
- Digital VLSI: low power digital design, RTL design using verilog, embedded memory design and access.
- RFIC: Components of wireless communication IC, RFIC architectures; design of Low-drop-out regulators (LDO), DC-DC convertors, PLLs, DLLs.

Research Projects

High-Speed Laser-forwarded Coherent Transcievers for Intra Data-Center Co-Packaged Optical(CPO) Interfaces, *University of California at Berkeley, USA* Aug. 2021 – Present.
Advisor: Prof. Vladimir Stojanovic

- Designed and taped out in GF45SPCLO process - a DP (Dual-Polarization) QAM-16 transciever module with a target data-rate of 448 Gbps/fiber/λ. The data-rate can be extended to 1.6 Tbps/fiber with the help of CWDM4 scheme.
- Proposed a new Mach-Zhender Modulator (MZM) architecture, which has much higher phae-shift efficiency compared to the conventional MZMs, to be used in the transmitter path.
- Developed an electro-optic co-optimization framework to minimize the overall tarnsceiver power consumption and optimize link performance.

Design of AMS Circuits Using Berkeley Analog Generator (BAG), *University of California at Berkeley, USA*
PI: Prof. Elad Alon Aug. 2020 – July. 2021

- Worked on designing a StrongARM latch comparator for a 200 Gbps MLSE receiver utilizing NRZ communication. Went through the entire flow of a generator based design (in BAG 3.0) starting from schematic generators and layout generators to testbench managers and measurement managers.
- Implemented portion of the digital back-end of the 200 Gbps MLSE RX (including the adaptation loop) in Chisel.

Master's dissertation on Current-Mode Full-Duplex Transceiver with Adaptive Equalization, *IIT Kharagpur, India* [*Thesis*][*Slides*] July. 2019 – Apr. 2020
Advisor: Prof. Pradip Mandal

- Designed a Current-Mode Full-Duplex transceiver arcitecture for high-speed chip-to-chip communication. A DIB (directional inverter-buffer)-g_m hybrid architecture has been used to dissociate the received signal from the transmitted signal with a very low error voltage. The transceiver also utilizes 2-tap Tx-FFE and a one-time adaptation scheme to set FFE tap coefficients depending on the channel loss characteristics. By utilizing a full-duplex transceiver architecture, this work proposes an elegant solution to the well-recognized problem of adapting Tx-FFE tap coefficients in high-speed equalization.
- Currently involved in laying out the design which will be followed by a full chip tape-out.

Bachelor's dissertation on Current-Integrating TIA RX with Adaptive Decision-Feedback Equalization (DFE), *IIT Kharagpur, India* [*Thesis*] [*Paper*][*Slides*] Sept. 2018 – April. 2019
Advisor: Prof. Pradip Mandal

- Proposed a regulated cascode based current -integrating TIA (RGC-CI-TIA) having a simulated voltage sensitivity of 1.2 mVppd and gain of 15. The proposed TIA achieves significantly lower power consumption compared to the conventional CGCI- TIA and shows a current efficiency of 100%. The RX also includes a current-integrating speculative decision feedback equalizer (DFE) whose tap coefficient is automatically adapted. The entire transceiver works at 5 Gbps data rate with an energy efficiency of 1.05 pJ/bit compensating a channel loss of 18 dB.

Design of Energy-Efficient Bidirectional Transceiver for Chip-to-Chip Communication, *IIT Kharagpur, India* [*Paper*][*Slides*]
Advisor: Prof. Pradip Mandal Feb. 2018 – Aug. 2018

- Proposed the design of a current-mode bidirectional transceiver for off-chip interconnects which deploys a feedforward equalization (FFE) scheme in transmitter for channel-loss compensation. The proposed transmitter makes use of a current-boosting driver (CBD) which boosts the pre-drive current, increasing the current-efficiency of the transmitter compared to the conventional CML driver. Moreover, compared to conventional passive terminated transceivers, the proposed transceiver utilizes an active termination in combination with a special biasing scheme, thereby making the termination impedance insensitive to process-voltage-temperature (PVT) variations. The entire architecture has been designed in 180 nm CMOS technology with a supply voltage of 1.8 V. Simulated power consumption in the transceiver pair is 6.4 mW with an energy efficiency of 1.28 pJ/bit while operating at 5 Gbps over 52-inch FR4 PCB trace having loss of 24.4 dB at Nyquist frequency.

Current-Mode Energy-Efficient Receiver with Active CTLE and DFE, *IIT Kharagpur, India* [*Slides*]
Advisor: Prof. Pradip Mandal Dec. 2017 – Feb. 2018

- Executed a thorough literature survey on state-of-the art receiver equalization techniques in high-speed wireline links, including continuous time linear equalization (CTLE), decision-feedback equalization (DFE) and their different variants.
- Proposed a new active CTLE receiver, which utilizes the basic principle of CTLE, however, obviates the need of a dedicated receiver before sending the data to the CTLE lowering the power consumption of the front-end. Designed a decision feedback equalizer (DFE) with 1-discrete-tap (DT) and 1-IIR tap which successfully cancels all the post-cursor ISI of the channel pulse response after getting equalized by the CTLE. The entire equalization scheme is able to compensate 22dB of loss offered by a 82-inch FR4 PCB trace, while working @ 2.5 Gbps data rate.

Design of Analog Front-end and ADC for Neural Data Acquisition, *Advanced VLSI Summer School, IIT Kharagpur, India* May. 2017 – July. 2017
Advisor: Dr. Mrigank Sharad

- Designed (in LTSpice) the analog fronted, consisting of a two stage double ended op-amp with dual CMFB technique followed by a variable gain amplifier, interfacing with multiple channels receiving neural data from human brain. The first op-amp, being very sensitive to noise, sized carefully to minimize the 1/f corner frequency and the noise floor.
- Designed a single-slope analog to digital converter(ADC) with capacitor based offset cancellation scheme, which is receiving the output of the analog front-end, sampling it with a TG based sampler and converting it into digital pulses whose width is proportional to the analog value.

Technical Skills

Programming

PYTHON, C, JAVA, MATLAB, VERILOG HDL, AVR Coding, ALP of μ-controllers

Software/Framework

Ansys Lumerical, Berkeley Photonic Generator (BPG), Berkeley Analog Generator (BAG), Chisel, Cadence Virtuoso, LTSpice, PSpice, Xilinx, Synopsis, Latex, Atmel Studio, Proteus, Solidworks, Keil μVision, Silvaco

Relevant Courses

UC Berkeley:

Analog Integrated Circuits (EE240A), Advanced Analog Integrated Circuits (EE240B), Introduction to Digital Design and Integrated Circuits (EECS251A), Integrated Circuit Devices (EE230A), Advanced Digital Integrated Circuits (EE241B), ASIC Lab (EECS251LA), Lightwave Devices (EE232), Fundamentals of Business (MBA209).

IIT Kharagpur:

- **Integrated Circuits:** Mixed Signal and RF Design, VLSI CAD, Digital VLSI Circuits, Analog VLSI Circuits, Architectural Design of ICs, VLSI Interconnects, Digital Electronic Circuits*, VLSI Engineering, Network Theory.
- **Communication:** Optical Communication, VLSI for Telecommunication, Modern Digital Communication Techniques, Digital Communication, Analog Communication.
- **Devices:** Semiconductor Device Modelling, Semiconductor Devices, Technology and Process Modelling.
- **Signal Processing:** Digital Signal Processing, Signals and Systems, Control Systems Engineering.
- **Others:** Micro-controller & Embedded Systems, RF & Microowave Engineering, Electromagnetic Engineering, Probability and Stochastic Processes, Algorithm Design and Analysis, Matrix Algebra, Graph theory and Algorithms, Programming and data structure, Basic Electrical technology.

Academic Distinctions

- Won Apple Watch SE as best student project award in EE241B (UCB), Spring 2021 (Sponsored by Apple Inc.)
- Won Apple AirPods pro for being a finalist in EE240A course project competition, Fall 2020 (Sponsored by Apple Inc.)
- Received best M.Tech project award at IIT Kharagpur for dissertation work in current-mode full-duplex transceiver.
- Awarded *VLSID fellowship* for attending VLSID 2019 conference held in New Delhi, India.
- Selected for *NTU-India Connect Program-2019* for pursuing a summer research internship at NTU, Singapore (Surrendered due to internship offer from Purdue University, USA).
- Selected in *Mitacs Globalink Program-2018* organized by Canadian government, (around 200 students selected from all over the world) for a summer research internship at *The University of British Columbia, Vancouver, Canada.*

- Selected for *DAAD-WISE scholarship*, awarded by German government for a research internship at Technical University of Munich (TUM), Germany.
- Currently *topper* of the specialization (Microelectronics & VLSI Design), holder of *rank-2* in the department (E&ECE) and *rank-4* in the institute with a cumulative GPA of 9.75/10.
- Secured a GPA of 10/10 in 7th and 8th semesters.
- Topper of the course in 1st, 3rd, 7th and 8th semesters.
- Recipient of *Merit-Cum-Means* (*MCM*) *scholarship* of IIT Kharagpur since 2015 (Given based on academic performance and financial requirements).
- Qualified in IIT-JEE (Advanced)-2015 with All India Rank-1665 (out of 1.5 million aspirants).
- Cracked *Indian Statistical Institute* (*ISI*) entrance examination (both written & interview)-2015 (60 students were selected from entire nation on the basis of excellence in mathematics and statistics).
- Cracked *Chennai Mathematical Institute* (*CMI*) entrance examination-2015 (around 100 students were selected from all over the nation).
- *KVPY fellowship* winner 2014-15 (Awarded by govt. of India based on scientific potential, with a nation-wide selectivity of 0.01% per year).